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ASSISTANT COMMISSIONER FOR PATENTS
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Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is the
[X] patent application of
[ ] continuation patent application of
[ ] divisional patent application of
[ ] continuation-in-part patent application of

Inventor(s)/Applicant Identifier: Thomas G. Adams and Randy R. Fuller

For: SYSTEM TIME CLOCK CAPTURE FOR COMPUTER SATELLITE RECEIVER

[X] This application claims priority from each of the following Application Nos./filing dates:
60/152,192 filed September 2, 1999
[ ] the disclosure(s) of which is (are) incorporated by reference.
[ ] Please amend this application by adding the following before the first sentence: "This application is a [ ] continuation [ ] continuation-in-part of and claims the benefit of U.S. Provisional Application No. 60/_____, filed _____, the disclosure of which is incorporated by reference."

Enclosed are:
[X] 6 page(s) of specification
[X] 4 page(s) of claims
[X] 1 page of Abstract
[X] 1 sheet(s) of [ ] formal [X] informal drawing(s).
[ ] An assignment of the invention to _____
[X] A [ ] signed [X] unsigned Declaration & Power of Attorney
[ ] A [ ] signed [ ] unsigned Declaration.
[ ] A Power of Attorney.
[ ] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27 [ ] is enclosed [ ] was filed in the prior application and small entity status is still proper and desired.
[ ] A certified copy of a _____ application.
[ ] Information Disclosure Statement under 37 CFR 1.97.
[ ] A petition to extend time to respond in the parent application.
[ ] Notification of change of [ ] power of attorney [ ] correspondence address filed in prior application.
[ ]

In view of the Unsigned Declaration as filed with this application and pursuant to 37 CFR §1.53(f), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

DO NOT CHARGE THE FILING FEE AT THIS TIME.

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Attorney Docket No.: 19927-000710US

PATENT APPLICATION

SYSTEM TIME CLOCK CAPTURE FOR COMPUTER SATELLITE RECEIVER

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SYSTEM TIME CLOCK CAPTURE FOR COMPUTER SATELLITE RECEIVER

This application claims the priority of U.S. Prov. Pat. Appl. No. 60/152,192, filed September 2, 1999, which is herein incorporated by reference for all purposes.

BACKGROUND OF THE INVENTION

The Digital Video Broadcast (DVB) standards and the Digital Satellite System (DSS) standards are designed for the delivery of digital video and digital audio "programs" to in-home set-top box appliances. More recently, interest has risen in using these standards for high bandwidth data delivery, for example, to personal computers for applications such as Internet access. The data broadcast may include, for example, internet protocol (IP) packets carrying electronic mail, world wide web content, and other data.

In data broadcast systems, various elementary streams of digital video, digital audio, and digital data typically are time-division multiplexed onto a single transport stream which is broadcast by way of a satellite transponder to multiple receivers. The elementary streams of information or data are generally packetized, as is the transport stream.

A receiver, for example, may be coupled to a personal computer. Such a receiver would receive the transport stream comprising the information, demultiplex elementary streams of digital video, digital audio, and/or data from the transport stream, and filter (select) those elementary streams destined for that receiver. The receiver further should be able to deliver the elementary streams to host memory of the personal computer for processing or display.

However, designing a receiver capable of demultiplexing, filtering, and delivering the elementary streams of information poses difficult problems and challenges. For example, critical timing constraints govern the delivery of elementary streams

containing digital video and digital audio programs. These critical timing constraints derive, for example, from the specific timing required for proper decoding and presentation of digital video frames on the host computer. Hence, the particular elementary streams must be demultiplexed, filtered, and delivered in real-time in such a way that these critical timing constraints are met. Moreover, accurate synchronization is required in order to meet these critical timing constraints.

SUMMARY OF THE INVENTION

In accordance with embodiments of the present invention, at the start of every transport packet reception, a first latch in the receiver captures a first system time clock (STC) timestamp. The first STC timestamp may be used to keep the receiver and the transmitter synchronized. In particular, if the transport packet contains a program clock reference (PCR) timestamp from the transmitter, then the PCR timestamp is compared with the first STC timestamp. Based on the comparison, control adjustment may be made to the STC frequency in order to maintain synchronization. In a preferred embodiment, this synchronization is accomplished using firmware in a transport controller within the receiver.

Further in accordance with the present invention, the contents of the transport packet are to be utilized by a decoder that is on a separate node of a host system from the receiver's node. The decoder may comprise hardware and/or software and may, for example, be part of an audio-visual or computer-network interface. To overcome the fact that the decoder and receiver are on separate nodes of the bus, a system and method is provided for the decoder to access the STC counter. The decoder captures a second STC timestamp by writing across the bus to a first register in a bus interface on the receiver. Writing to the first register causes the second STC timestamp to be latched in a second register in the bus interface. The decoder may then complete capture of the second STC timestamp by retrieving it over the bus. The second STC timestamp may be compared to the last PCR timestamp received to provide an accurate indication of elapsed time since receipt of the last PCR timestamp.

Synchronization between the decoder and the receiver is maintained with a system timestamp captured by the decoder. This system timestamp is adjusted with a scaled offset based on a message delay time between the decoder and the receiver.

A further understanding of the nature and advantages of the present invention may be realized by reference to the remaining portions of the specification and the drawings.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a schematic diagram including a system in accordance with a preferred embodiment of the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

Fig. 1 is a schematic diagram including a system in accordance with a preferred embodiment of the present invention. A satellite transponder 102 transmits a signal carrying a transport stream to multiple receiver dishes 104, one of which is shown in Fig. 1. Receiver dish 104 in Fig. 1 is coupled to a host computer system 106 by way of a link interface 111 on a receiver circuit 108. Receiver circuit 108 may comprise an integrated circuit, a circuit board having the different receiver components attached thereto, or any other suitable circuit design or configuration.

Receiver circuit 108 includes a local bus 110 to which is coupled a transport controller 112, a local CPU 114, and local memory 116. Transport controller 112 receives the transport stream from link interface 111 and handles low-level transport stream parsing. Local CPU 114 comprises a microcontroller that controls operations on receiver circuit 108. Local memory 116 comprises memory such as static RAM, dynamic RAM, or ROM located on receiver circuit 108.

A bus interface 118 couples local bus 110 on receiver circuit 108 to a host system bus 120 of host computer 106. In a preferred embodiment, host system bus 120 comprises a PCI bus, and bus interface 118 comprises a PCI interface. Also coupled to host system bus 120 are a host CPU 122, host memory 124, an audio-visual interface 126,

and a network interface 130, among other components. Host CPU 122 comprises the microprocessor of host computer 106, and host memory 124 comprises memory of host computer 106. Audio-visual interface 126 comprises a graphics interface that is coupled to an audio-visual system 128. Audio-visual system 128 may include, for example, speakers and a CRT monitor or a flat panel display. Network interface 130 comprises a network interface card which is coupled to a local area network (LAN) 131 which is in turn coupled to one or more networked computer system(s) 132. For example, network interface 130 may comprise an ethernet card, LAN 131 may comprise an ethernet network, and networked computer system(s) 132 may comprise personal computers.

The present invention relates to timing information based on a transmitter System Time Clock (STC) counter that is periodically inserted by the transmitter into a transport stream. There are various circumstances in which it is highly desirable to account for the delay between reception of a packet from the transmitter and actual applications using that packet. This is the case, for example, in applications where a direct memory access engine is used to transfer elementary streams from the receiver, such as described in the concurrently filed and commonly assigned application entitled "MULTITHREADED DIRECT MEMORY ACCESS ENGINE FOR BROADCAST DATA DEMULTIPLEX OPERATIONS," (Attorney Docket No. 19927-000510US) having Thomas Gene Adams and Gene Maine as coinventors, which is herein incorporated by reference for all purposes. Such applications may also include flexibile media access control as described in the concurrently filed and commonly assigned application entitled "FLEXIBLE MEDIA ACCESS CONTROL AND SECTION FILTER HARDWARE ENGINE FOR SATELLITE DATA RECEIVER," (Attorney Docket No. 19927-000610US) having Thomas G. Adams and Randy R. Fuller as coinventors, which is also herein incorporated by reference for all purposes. Since there is considerable variability in the delay through the steps of demultiplexing the elementary streams and performing the direct memory access through the firmware and software layers, it is desirable to use the calculation of the delay to synchronize the operations.

Receiver circuit 108 receives the transport stream and utilizes the injected timing information for purposes of synchronizing a receiver System Time Clock (STC) counter with the transmitter STC counter. In accordance with a preferred embodiment, the timing information based on the transmitter STC clock is inserted into a special

segment of a MPEG-2 transport packet that is called an "adaptation field." In particular, the adaptation field includes a Program Clock Reference (PCR) timestamp, which is a sampled value of the transmitter STC counter. When a packet containing a PCR value is initially received, it is timestamped with its local timer value. As the packets are passed to various drivers for processing, uncertainties in the hardware and software timing accumulate. It is therefore not possible simply to receive a PCR value from the received data stream, pass it between host drivers, and use it for decoder and presentation timing. According to embodiments of the invention, the PCR timestamp is instead referenced to a time base accessible to all host software elements. This system time value is referred to herein as "system time," with a latched value of system time being referred to as a "system timestamp." Various methods may be used to generate system time, including the use of performance timers or other computer timing references, provided that all host drivers have access to the same system time reference so that system timestamps may be compared.

Thus, in accordance with one embodiment of the present invention, at the start of every transport packet reception, a first latch in receiver circuit 108 captures a first STC timestamp. The first STC timestamp may be used to keep the receiver and the transmitter synchronized. In particular, if the transport packet contains a PCR timestamp from the transmitter, then the PCR timestamp is compared with the first STC timestamp. Based on the comparison, control adjustment may be made to the STC frequency in order to maintain synchronization. In a preferred embodiment, this synchronization is accomplished using firmware in a transport controller within receiver circuit 108.

Further in accordance with the present invention, the contents of the transport packet are to be utilized by a decoder that is on a separate node of a host system bus 120 from the receiver's node. The decoder may comprise hardware and/or software and may, for example, be part of an audio-visual interface 126. In an alternative embodiment, the decoder is part of a computer network interface 130. To overcome the fact that the decoder and receiver are on separate nodes of bus 120, a system and method is provided for the decoder to access the STC counter. The decoder captures a second STC timestamp by writing across bus 120 to a first register in a bus interface 118 on receiver circuit 108. Writing to the first register causes the second STC timestamp to be latched in a second register in bus interface 118. The decoder may then complete capture

of the second STC timestamp by retrieving it over bus 120. The second STC timestamp may be compared to the last PCR timestamp received to provide an accurate indication of elapsed time since receipt of the last PCR timestamp.

The time between PCR reception and the decoder capturing the system timestamp may be quite variable. This delay time can be determined accurately by using the receiver and decoder timestamps. The system timestamp is then adjusted to account for this delay:

$$T'_{system} = T_{system} - x(T_{decoder} - T_{receiver}).$$

The adjusted system timestamp is calculated by offsetting the system timestamp by a scaled message delay. The message delay is the difference between the decoder timestamp $T_{decoder}$ and the receiver timestamp $T_{receiver}$. This message delay is scaled by the scale factor x to take into account that system time may be referenced to a different clock reference than the decoder and receiver timestamps. If they are referenced to the same clock reference, the scale factor may take the value $x = 1$. However, in circumstances, for example, where system time is extracted from a personal computer clock and the decoder and receiver times are extracted from the receiver reference clock, the scale factor may be nonzero.

Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative embodiments, and equivalents may be used without departing from the spirit of the invention. Accordingly, the above description should not be taken as limiting the scope of the invention, which is defined in the following claims.

WHAT IS CLAIMED IS:

1. A method for a receiver to provide access to a system time clock (STC) to a decoder, the method comprising:

(a) receiving data from the decoder into a first register in a bus interface, where the bus interface couples the receiver to a bus;

(b) latching a timestamp of the STC into a second register in the bus interface after receiving the data; and

(c) providing the timestamp to the decoder by way of the second register.

2. The method according to claim 1 wherein the decoder is part of an audio-visual interface.

3. The method according to claim 1 wherein the decoder is part of a computer network interface.

4. A method for synchronizing a digital video system including a transmitter, a receiver, and a decoder, the method comprising:

(a) receiving a first transport packet from the transmitter;

(b) capturing a first system time clock (STC) timestamp at a start of receiving the first transport packet, the first STC timestamp being captured into a latch;

(c) obtaining a program clock reference (PCR) timestamp from the transport packet;

(d) comparing the first STC timestamp to the PCR timestamp to generate a comparison result; and

(e) adjusting an STC frequency based on the comparison result in order to maintain synchronization between the receiver and the transmitter.

5. The method according to claim 4 wherein the method is accomplished in the receiver.

6. The method according to claim 4 further comprising:

(a) capturing a system timestamp with the decoder; and

(b) adjusting the system timestamp with a scaled offset based on a message delay time between the decoder and the receiver to maintain synchronization between the decoder and the receiver.

7. The method according to claim 4 further comprising:

(a) receiving data from the decoder into a first register in a bus interface, wherein the decoder is coupled to a communication bus, and where the bus interface couples the receiver to the communication bus;

(b) latching a second STC timestamp into a second register in the bus interface after receiving the data from the decoder; and

(c) providing the second STC timestamp to the decoder by way of the second register.

8. The method according to claim 4 wherein the decoder is part of an audio-visual interface.

9. The method according to claim 4 wherein the decoder is part of a computer network interface.

10. A system for a receiver to provide access to a system time clock (STC) to a decoder, the system comprising:

(a) a communication bus coupled to the decoder;

(b) a bus interface in the receiver, the bus interface coupling the receiver to the communication bus;

(c) a first register in the bus interface, the first register being adapted to receive data across the communication bus from the decoder; and

(d) a second register in the bus interface, the second register being adapted to latch a timestamp of the STC after the first register receives the data and to provide the timestamp to the decoder by way of the communication bus.

11. The system according to claim 10 wherein the decoder is part of an audio-visual interface.

12. The system according to claim 10 wherein the decoder is part of a computer network interface.

13. A system for synchronizing a digital video transmitter, receiver, and decoder, the system comprising:

(a) a parser adapted to obtain a program clock reference (PCR) timestamp from a first transport packet, the first transport packet including the PCR timestamp;

(b) a first latch coupled to the parser, the first latch being adapted to capture a first system time clock (STC) timestamp near a beginning of receipt of a first transport packet by the receiver;

(c) a comparison device coupled to the parser and to the latch, the comparison device being configured to compare the STC timestamp to the PCR timestamp so as to generate a comparison result; and

(d) a first adjuster coupled to the comparison device, the first adjuster being adapted to adjust a frequency of the system time clock based on the comparison result in order to maintain the synchronization between the receiver and the transmitter.

14. The system according to claim 13 wherein the parser and latch are in the receiver.

15. The system according to claim 13 further comprising:

(a) a second latch in the decoder, the second latch being adapted to capture a system timestamp; and

(b) a second adjuster coupled to the decoder, the second adjuster being adapted to adjust the system timestamp with a scaled offset based on a message delay time between the decoder and the receiver to maintain synchronization between the decoder and the receiver.

16. The system according to claim 13 further comprising:

(a) a first register in a bus interface, the first register being adapted to receive data from the decoder, where the decoder is coupled to a communication bus, and where the bus interface couples the receiver to the communication bus; and

(b) a second register in the bus interface, the second register being adapted to latch a second STC timestamp after the first register receives the data from the decoder, wherein the second STC timestamp is provided to the decoder by way of the second register.

17. The system according to claim 13 wherein the decoder is part of an audio-visual interface.

18. The system according to claim 13 wherein the decoder is part of a computer network interface.

SYSTEM TIME CLOCK CAPTURE FOR COMPUTER SATELLITE RECEIVER

ABSTRACT OF THE DISCLOSURE

A method and system are provided for synchronizing a digital video system that includes a transmitter, a receiver, and a decoder. A transport packet is received from the transmitter. At the start of receiving the transport packet, a system time clock timestamp is captured. A program clock reference timestamp is also obtained from the transport packet and is compared with the system time clock timestamp.

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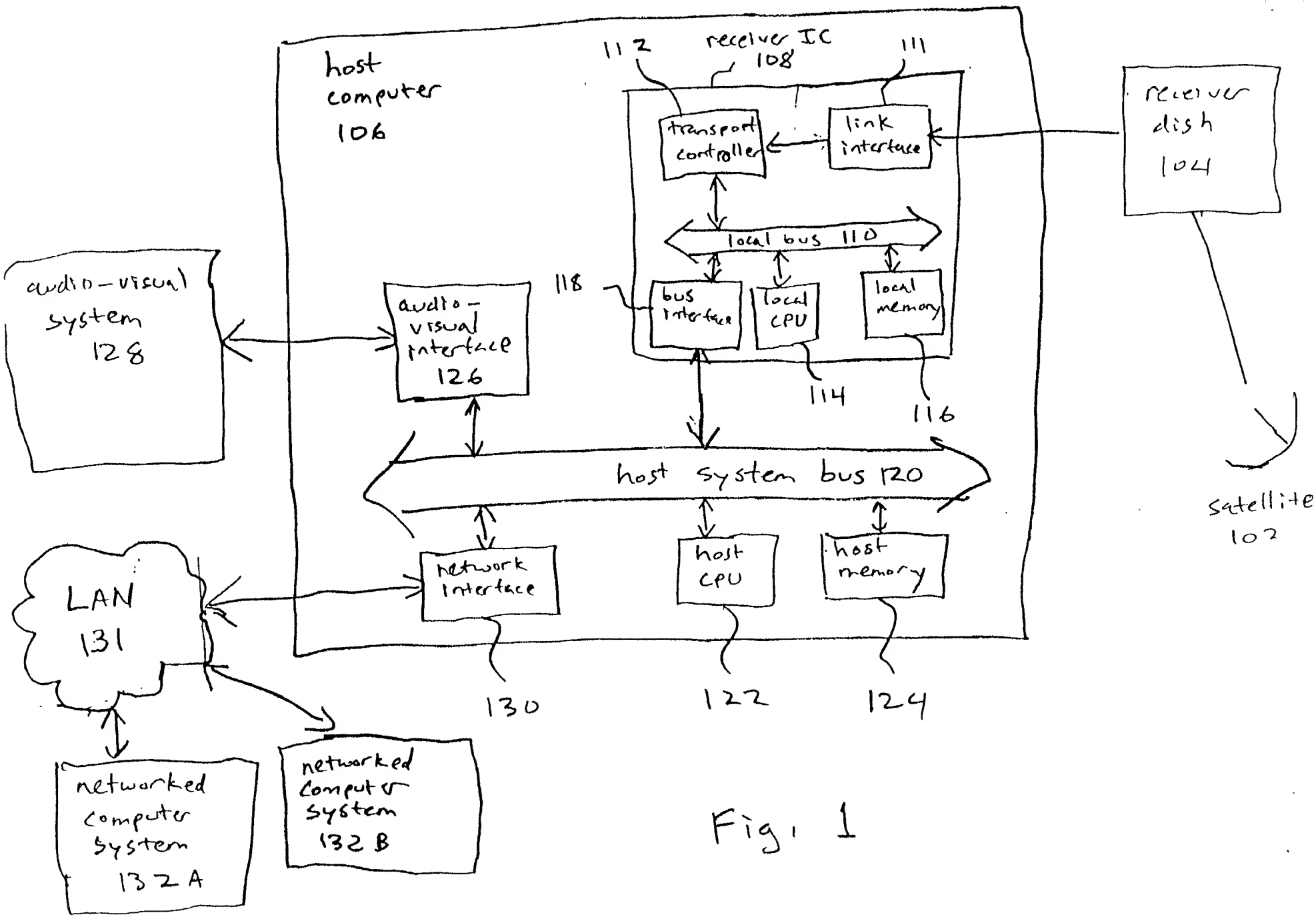

Fig. 1

DECLARATION

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SYSTEM TIME CLOCK CAPTURE FOR COMPUTER SATELLITE RECEIVER** the specification of which __X__ is attached hereto or ____ was filed on _____ as Application No. _____ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/152,192	09/02/99

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

Full Name of Inventor 1:	Last Name: **ADAMS**	First Name: **THOMAS**	Middle Name or Initial: **G**	
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I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1	Signature of Inventor 2
Thomas G Adams	Randy R Fuller
Date	Date

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